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Design of Multioctave High-Efficiency Power Amplifiers Using Stochastic Reduced Order Models

Yuan Zhuang, *Graduate Student Member, IEEE*, Zhouxiang Fei, Anqi Chen, Yi Huang, *Senior Member, IEEE,* Khondker Rabbi, and Jiafeng Zhou

***Abstract*— This paper presents a novel general design method of frequency varying impedance matching. The method is applied to design of a broadband high-efficiency power amplifier (PA). The proposed method defines the optimal impedance regions of a PA at several frequency sections over the operational frequency band. These regions contain the impedances that can achieve a high output power and a high-power added efficiency (PAE) simultaneously. A low-pass LC-ladder circuit is selected as the matching network (MN). The element values of the MN can be obtained using a synthesizing method based on stochastic reduced order models and Voronoi partition. The MN provides desired impedance in the predefined optimal impedance region at each frequency section. Thus, optimal output power and PAE of the PA can be achieved. To validate the proposed method, two eighth-order low-pass LC-ladder networks are designed as the input and output MNs, respectively. A gallium nitride (GaN) HEMT from Cree is employed as the active device. Packaging parasitic of the transistor has been taken into account. A PA is designed, fabricated, and measured. The measurement results show that the PA can achieve P1 dB PAE of better than 60% over a fractional bandwidth of 160% (0.2–1.8 GHz). The output power is 42–45 dBm (16–32 W), and the gain is 12–15 dB. The performance of the PA outperforms existing broadband high-efficiency PAs in many aspects, which demonstrates the excellence of the proposed method.**

***Index Terms*— Broadband power amplifier (PA), gallium nitride (GaN) high electron mobility transistor (HEMT), high-efficiency PA, PA, stochastic reduced order model (SROM), voronoi partition, wideband matching network (MN).**

I. Introduction

POWER amplifiers (PAs) are essential devices of many communication systems. The features of a PA regarding the bandwidth, power gain, linearity, output power, and power added efficiency (PAE) could significantly affect the overall performance of the system. A high-power, high-efficiency broadband PA is in high demand by the industry and market. Consequently, a lot of research efforts have been made in this area to achieve better performance.

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The authors are with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, L69 3GJ, U.K. (e-mail: sgyzhua2@liverpool.ac.uk; zhouxiang.fei@liverpool.ac.uk; sgachen@liv.ac.uk; yi.huang@liverpool.ac.uk; K.Rabbi@liverpool.ac.uk; jiafeng.zhou@liverpool.ac.uk).

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To achieve a high-efficiency PA, designs reported in the literature have adopted techniques such as class E [1]–[8], class D [9], [10], class F/F^{-1} [11]–[16], and Doherty structures [17]–[21]. Although these methods enhance the efficiency of a PA, the requirement on accurate waveform engineering would restrict the bandwidth. Hence, to broaden the bandwidth of a PA, some designs such as [22]–[25] use a filter-type matching network (MN) to match the fixed optimal impedance at the center frequency of the PA over a wide bandwidth. This technique achieves the optimal performance at the center frequency and compromises the performance at other frequencies over the band at a reasonable level. However, this method requires the optimal impedance across the band to be relatively close to each other. Therefore, this approach is not applicable for the design where the optimal impedance is not close to each other, which is almost always the case in a multioctave PA design.

Conventional computer-aided design (CAD) tools can be used for this kind of problems. However, CAD optimizers require good initial element values to start with [17], [25]. Methods such as the real frequency technique [38] and Bayesian optimization [37] can be applied to solve the problem. However, a proper initial guess or data training will be required for such optimizers which can be very time consuming [39].

This paper presents a simple and effective method for the design of broadband high-efficiency PAs. This new approach divides the wide frequency band into several frequency sections. At each frequency section, an optimal impedance region will be obtained, where the output power and PAE of the PA can be optimized. The main advantage of the proposed method is that the MN can be obtained using the Stochastic reduced order model (SROM) method and Voronoi partition directly. No initial guess or data training is required. This paper is organized as follows. The design method is detailed and explained in Section II, including how to define the optimal impedance regions and how to match the impedance with a low-pass LC-ladder network. Source-pull/load-pull simulations are performed to obtain the frequency-dependent optimal impedance regions for the PA in Section II. As an example, the proposed design method is used to design an MN in Section III, and the MN is fabricated and measured to validate the method. In Section IV, A 25-W Cree GaN HEMT CGH40025F is used to design a PA, whose package

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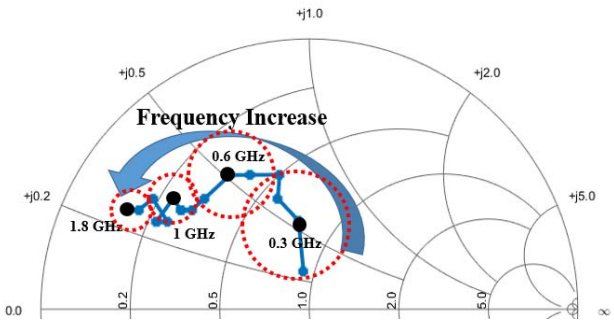

Fig. 1. PAE optimal impedance of a CGH40025F transistor at different frequencies (0.3, 0.6, 1, and 1.8 GHz).

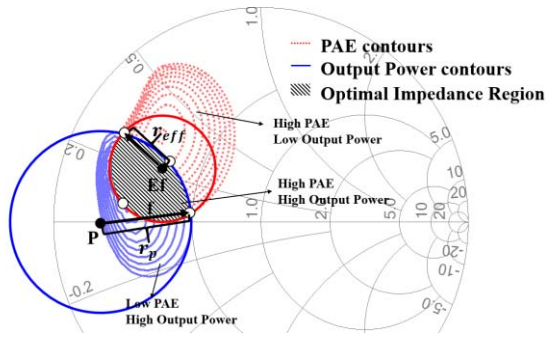

Fig. 2. PAE contours, output power contours, and the definition of an optimal impedance region at 1 GHz of a CGH40025F.

parasitic is carefully analyzed. The measurement results of the PA are presented and discussed. Conclusions are finally drawn in Section V.

II. Proposed Design Method

A. Broadband High-Power High-Efficiency PA Analysis

The impedances presented to the gate and drain of a transistor could significantly affect the performance of a PA. Therefore, MNs with desired impedance are required for the transistor to achieve high performance. For broadband PA design, the impedances to achieve high PAE or high output power are usually different at different frequencies. Source-pull and load-pull techniques can be applied to find the optimal impedances for the PAE and output power. Fig. 1 shows the PAE contours from 0.2 to 1.8 GHz of a CGH40025F transistor in a Smith Chart. The contours vary with frequency and are quite different from each other. Consequently, to design an efficient high-power PA over an ultra-wide bandwidth, the optimal impedances should be implemented at different frequency regions across the band, instead of at the center frequency.

It is very common that the output power and PAE contours are not identical, as shown in Fig. 2. The impedance to maximize the PAE could limit the output power and vice versa. An optimal impedance region at each frequency region should be defined, which contains the impedance values that allows the PA to achieve high performance with a PAE and an output power better than the lowest acceptable levels, as shown in Fig. 2.

B. Frequency-Dependent Optimal Impedance Regions

The design methods reported in [7], [23], and [24] that used the optimal impedance at the center frequency for the whole frequency band may not be the best for a multioctave PA design. The entire bandwidth can be separated into several frequency sections. The optimal impedance region at the center frequency of each frequency section can be selected to represent the optimal impedance of this frequency section. In the literature, it is very common that designers simply divide the frequency band in to several sections evenly such as [2], [22], [23], and [25]. It is very important to notice that for an ultra-wideband design, the variation of the optimal impedance across the band is not uniform. As shown in Fig. 1, the PAE optimal impedance of a CGH40025F is simulated from 0.2 to 1.8 GHz with a step of 0.1 GHz. As shown in Fig. 1, the optimal impedances are getting closer at higher frequencies.

Hence, more frequency sections should be set at lower frequencies to ensure that the optimal impedance at the center frequency of the section can maintain the desired performance over the corresponding frequency section. Thus, the separation of the frequency band should be based on the variation of the optimal impedances across the bandwidth.

The optimal impedance regions can be chosen based on the desired features of a PA such as the power gain, linearity, output power, and PAE. In this paper, high output power and high PAE are the main design targets. The optimal impedance regions across the band are defined and modeled as follows:

1) Divide the entire operation bandwidth into k frequency sections. The number of frequency sections depends on the bandwidth and the variation of optimal impedances at different frequencies.
2) For each frequency section, the output power, and PAE contours of the center frequency of this section can be obtained via source-pull/load-pull simulation. The boundary of the contours is defined by the lowest output power and PAE acceptable for the design. The overlap region of output power and PAE contours is selected to be the optimal impedance region (shaded area in Fig. 2). If the contours do not overlap, a sacrifice is necessary to extend the PAE or output power contours until they have an overlap region (if the output power is the priority concern, the lowest acceptable PAE level should be reduced and vice versa).
3) For mathematical convenience, the optimal impedance region can be approximated by two circles, as shown in Fig. 2. Any three noncollinear points can define the circumference of one circle, and one circle only. Two intercept points of the PAE and output power contour boundaries and another point on the PAE contour boundary inside the output power contour will define the PAE circle. The circle of output power can be defined likewise. Then the overlap region of the PAE and output power circles is defined as the optimal impedance region. The impedance values of the region can be expressed as a function of frequency as

$$\begin{cases} d_P(\omega_x) \le r_P(\omega_x) \\ d_{\mathrm{Eff}}(\omega_x) \le r_{\mathrm{Eff}}(\omega_x) \end{cases} \tag{1}$$

where $\omega_x = 2\pi f_x$, $x = 1, 2, .., k$, where k is the number of frequency sections. d_P and d_{Eff} are the Euclidean

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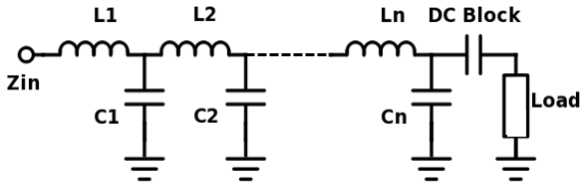

Fig. 3. Low-pass *LC*-ladder MN with a DC block.

distance from the impedance point to the center of the PAE and output power circles, r_P and r_{Eff} are the radius of the PAE and output power circles, respectively.

The optimal impedance region at each frequency section across the desired bandwidth can be obtained as described above. The input impedance of the MN seen by the transistor at each frequency section should be constrained to the corresponding optimal impedance region. This approach will enable the output power and PAE of a PA to be better than the predefined level over the whole operational band. Also, some other features of a PA such as noise figure or gain can be included to define the optimal region as well if required.

C. Synthesis of the Matching Networks

Once the optimal impedance regions across the entire bandwidth are defined, the task resides in realizing the desired impedances using a proper circuit topology. A low-pass *LC*-ladder MN with a dc block capacitor as shown in Fig. 3 is chosen as the MN due to its desired in-band and out-of-band behavior as analyzed in [6] and [27]. The input impedance of the MN can be described as a function of frequency and element values. First, the MN can be treated as a cascaded structure of several *LC* sections. The ABCD matrix of the MN can be expressed [28] as

$$\begin{bmatrix} A(\omega_x) & B(\omega_x) \\ C(\omega_x) & D(\omega_x) \end{bmatrix}_{LC} = \prod_{i=1}^{n} \begin{bmatrix} 1-\omega_x^2 L_i C_i & j\omega_x L_i \\ j\omega_x C_i & 1 \end{bmatrix} \quad (2)$$

where n is the number of *LC*-ladder sections used in the network, L_i and C_i are the ith inductor and capacitor values. The input impedance Z_{in} of the MN can be described [28] by

$$Z_{\text{in}}(\omega_x) = \frac{Z_{\text{load}} * A(\omega_x) + B(\omega_x)}{Z_{\text{load}} * C(\omega_x) + D(\omega_x)} \quad (3)$$

where A, B, C, and D are the values obtained in (2) and Z_{load} is the load resistance of the MN, typically 50 Ω for most applications. With the expression of (3), the input impedance at each frequency section of the MN can be obtained once the *LC* values are known.

The problem now resides in choosing proper *LC* values to ensure Z_{in} of the MN at each frequency section is inside the optimal impedance regions defined by (1). The MN should enable the device to achieve optimal performance across the whole bandwidth. Although some commercially available software such as ADS and AWR are useful in broadband impedance matching, the built-in optimizer is limited by high dimensional variables or strict optimization goals. Another solution is to use the Monte Carlo (MC) simulation to search all the possible values of the *LC* components exhaustively, and then select the *LC* values fulfilling the design requirements. The MC method requires massive calculation due to many possible *LC* values to be examined. Alternatively, the *LC* values can be obtained in a more efficient way. The ideal is inspired by a novel statistical approach referred to as the SROM method [36]. Unlike MC, the SROM method only needs to examine a very small number of samples, but produces the results almost as accurate as that of the MC method. The SROM method is applied to the Voronoi partition [29] to divide the possible values of variables into several regions based on the statistical properties of the variables. Then, a sample at the centroid of each region is used to represent all the points in this region. An example is shown in Fig. 4 illustrating the Voronoi partition of a two-dimension variable. This method only looks at representative samples obtained using the Voronoi partition, but the effect is nearly equivalent to the MC method by checking all the possible samples. Hence, in this paper, the Voronoi partition (the nucleus of the SROM method) is used to choose the *LC* values for MNs efficiently.

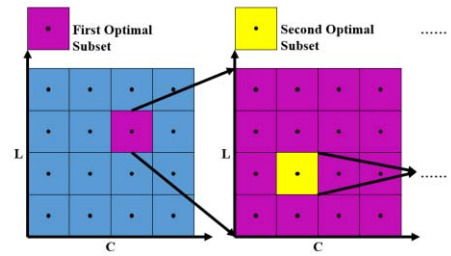

Fig. 4. Illustration of the Voronoi partition and the optimal subset. (A two-dimension diagram is shown as an example. In a real design the number of variable dimensions may be higher).

To perform the Voronoi partition, the input variable needs to be known beforehand. The dimension of the input variable is equal to the number of variables, e.g., the number of L and C components in the MN. In this way, each sample in the input variable contains a set of *LC* values for a possible realization of the MN. The Voronoi partition of the components values for the proposed MN can be realized in the following steps.

1) It can be assumed that the number of *LC* sections used in the MN is n (i.e., n inductors and n capacitors). Let $\boldsymbol{X}$ be an input variable with a dimension of $2n$. Each dimension of $\boldsymbol{X}$ describes a set of component values (either L or C) in the circuit, i.e., $\boldsymbol{X} = [L_1, L_2, \ldots, L_n, C_1, C_2, \ldots, C_n]$. The Voronoi partition of the input variable $\boldsymbol{X}$ with $2n$ dimensions can be constructed as shown in Fig. 4 (a two-dimension diagram is shown as an example).
2) Divide the range of the possible L or C component values into m Voronoi regions for each dimension of X, based on the distribution in the variation range. Then select one sample at each section as a representative following the distribution of the component value between its upper and lower limits. The value of m can be heuristically chosen depending on the affordable number of trials. Theoretically, a greater value of m yields a

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higher probability of obtaining the optimum solution. In practice, the solution that meets the design requirement can be obtained even using a small value of m.

3) The m samples of $\boldsymbol{X}$ are obtained as: the ith ($1 \leq i \leq m$) sample of $\boldsymbol{X}$ contains $2n$ values (i.e., from the ith sample of L_1 to the ith sample of C_n). Each element in sample $(\tilde{\boldsymbol{x}}^{(1)}, \ldots, \tilde{\boldsymbol{x}}^{(m)})$ should be the centroid of the ith Voronoi region [35]. Now, the infinite number of possible values for X is reduced to $2n \times m$ samples.
4) With the LC values in the obtained samples from Voronoi partition, (2) and (3) can be used to calculate the corresponding input impedance $Z_{\text{in}}(\omega_x)$ of each sample. The shortest Euclidean distance from the input impedance to the output power and PAE contour $d_P^{(m)}(\omega_x)$ and $d_{\text{Eff}}^{(m)}(\omega_x)$ can be calculated. If $d_P^{(m)}(\omega_x)/r_P(\omega_x) \leq 1$ and $d_{\text{Eff}}^{(m)}(\omega_x)/r_{\text{Eff}}(\omega_x) \leq 1$, it indicates that the input impedances of the mth sample are in the optimal impedance regions over the desired band. The values in this sample can be used to synthesize the MN.
5) If no subset can meet the requirements, the shortest Euclidean distance from the input impedance to the optimal impedance region should be calculated. The matching quality of the sample can be evaluated by

$$\Lambda^{(m)} = \sum_{i=1}^{k} |d_{\text{in}}^{(m)}(\omega_x)|^2 \tag{4}$$

where the $d_{\text{in}}^{(m)}(\omega_x)$ is the shortest Euclidean distance from the input impedance of the mth sample at xth frequency section to the corresponding optimal impedance region. The mth sample that has the minimum $\Lambda^{(m)}$ will be selected as the optimum subset for further optimization. Repeat the Voronoi partition for the optimum subset as shown in Fig. 4 until the requirements are satisfied. If the requirements cannot be satisfied after repeating the partition, it indicates that the obligation cannot be met with the current order of the MN. Herein, it will be necessary to increase the order of the MN or decrease the lowest limits of the output power and PAE and start again from Step 1. A practical design procedure is shown in Section III.

Using the proposed method, only $2n \times m$ samples need to be checked, which significantly reduced the calculation complexity. The solution of the LC values obtained using this method may not be the best one because the calculation cannot include every single possible combination of LC values. However, it is sufficient to obtain a solution that could ensure the input impedance at each frequency section is inside the corresponding optimal impedance region. An infinitely small separation of the LC value samples and an infinite order of the MN will offer a very accurate result, whereas the implementation will be very computationally intensive [36]. Consequently, the tradeoff between accuracy and computation cost should be considered when determining the size of the separation and the number of iterations.

III. Design and Implementation of the Matching Networks

In this section, a PA covering the frequency band of 0.2 to 1.8 GHz is designed to verify the proposed method. The output power of the PA is expected to be higher than 42 dBm across the band, and the PAE at the 1-dB compression point is desired to be better than 60%.

A. Load–Pull Simulation

Gallium nitride (GaN) high electron mobility transistors (HEMTs) have widely been adopted in broadband high-efficiency PA designs [6], [16], [17], [25]. An unmatched 25-W Cree GaN HEMT CGH40025F is chosen for this PA design. This transistor has a breakdown voltage up to 84 V and a saturation drain current of 5.4 A. Intrinsic waveforms of the transistor are simulated by using CAD tools to investigate the operation of the transistor. The transistor is sealed in the Cree 400166 package. To minimize the parasitic effect introduced by the package, the intrinsic and extrinsic elements are calculated using the method provided in [6] and [30]. These parasitic effects should be included in source–pull/load–pull simulations to predict the optimal impedance regions of the transistor.

The source–pull/load–pull simulation was carried out to find the optimal impedance. The simulation is performed using ADS with the transistor model provided by the manufacturer. The device is biased at 28-V drain voltage and −3.2-V gate voltage ($I_{\text{DQ}} = 50$ mA). The input power is 30 dBm.

The desired operation bandwidth in thispaper is 0.2–1.8 GHz. The operational band is divided into four frequency sections as discussed and shown in Fig. 1. Then load–pull simulation is conducted to obtain the output power and PAE contours. The design goals require an output power higher than 42 dBm and a PAE better than 60% across the band. The optimal impedance regions which satisfy the design goals are defined using the method in Section II and then extracted from the load-pull simulation, as shown in Fig. 5. Then the method described in Section II was used to design the output MN (OMN). The input MN (IMN) can be designed via the same procedure.

B. OMN Design

This section presents details of the design and implementation of the OMN using the method above. First, the order of the LC sections for the OMN should be determined [27]. A wider bandwidth and a greater range of impedance variations usually require higher order designs. On the other hand, a higher order MN is typically lossier. The design process starts with the number of the LC sections $n = 1$. Then n is increased until the requirement is satisfied. It was found by calculation [27] that when $n = 4$ (for an eighth-order LC network), the impedance at each frequency section is inside the corresponding optimal impedance region. A 33-pF capacitor is added as a dc block at the end of the LC-ladder network and considered in the circuit optimization. The MN circuit is shown in Fig. 3.

The Voronoi partition of the LC values are constructed as $\boldsymbol{X} = [L_1, L_2, \ldots, L_n, C_1, C_2, \ldots, C_n]$. To define the Voronoi

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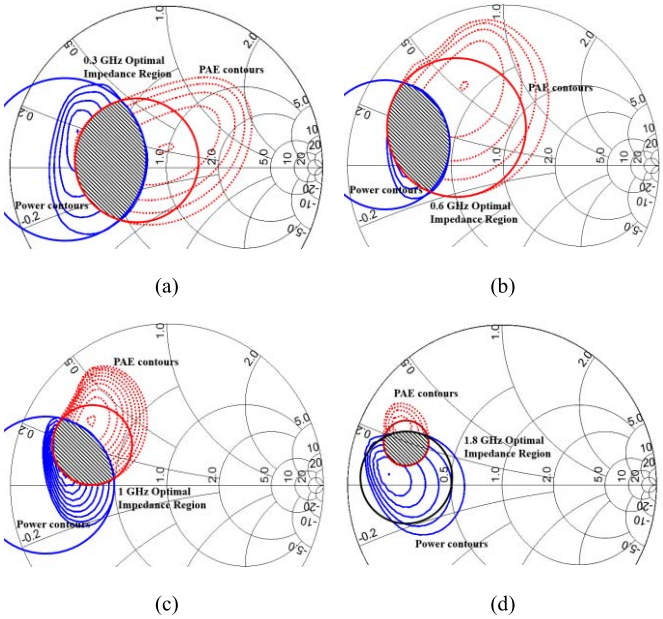

Fig. 5. Simulation results of optimal impedance regions at (a) 0.3 GHz, (b) 0.6 GHz, (c) 1 GHz, and (d) 1.8 GHz.

partition, the elements of L and C are uniformly divided into several samples from 0 to 30 nH and 0 to 30 pF into 16 steps, respectively. The greatest values of the inductances and capacitances are high enough for the operational frequency range. The number of samples m is selected to be 16. Then the input impedance at each frequency section for all samples of LC combinations were computed by (2) and (3). Then an investigation was conducted to check whether the corresponding input impedances of the samples are inside the predefined optimal impedance regions. Since no sample can satisfy the design goal, the matching quality of was calculated by (4). The optimal subset with $X = [2\text{ nH}, 2\text{ nH}, 2\text{ nH}, 4\text{ nH}, 2\text{ pF}, 2\text{ pF}, 6\text{ pF}, 2\text{ pF}]$ is found to have the best matching quality and selected for further optimization. The values of the selected optimal subset are divided again. The process was repeated until the matching requirements have been meet.

For this design, the optimum subset containing the LC combination that satisfies the design goals has been found in the third-round Voronoi partition. All the three optimal subsets selected by the process are shown along with the corresponding LC element values in Table I. The input impedances realized by each optimal subset and the predefined optimal impedance regions are illustrated in Figs. 6–8. The input impedances of the second-round subset are inside the optimal impedance regions except the impedance at 1.8 GHz. With the third-round optimal subset, the input impedance at each frequency section is constrained in the corresponding optimal impedance region, which will ensure that the design goals will be satisfied.

C. OMN Implementation

Since the availability of high-quality inductors and capacitors to implement the design is quite limited, a distributed element version of the OMN is designed and fabricated. All the LC components are realized by transmission lines expect the dc block capacitor [28]. The inductors are implemented by high-impedance transmission lines while the capacitors are realized by low-impedance open stubs. It should be mentioned that the effects of shunt susceptance of the high-impedance lines and the series reactance of the low-impedance stubs should also be considered [34]. The lengths of inductive lines

TABLE I

VALUES OF LC ELEMENTS FOR EACH OPTIMAL SUBSET

Optimal Subset	L (nH)				C (pF)			
	L_1	L_2	L_3	L_4	C_1	C_2	C_3	C_4
1	2	2	2	4	2	2	6	2
2	1	2	2	4	1	2	5	2
3	0.5	1.6	1.9	4.6	1.1	2.6	4.6	2.7

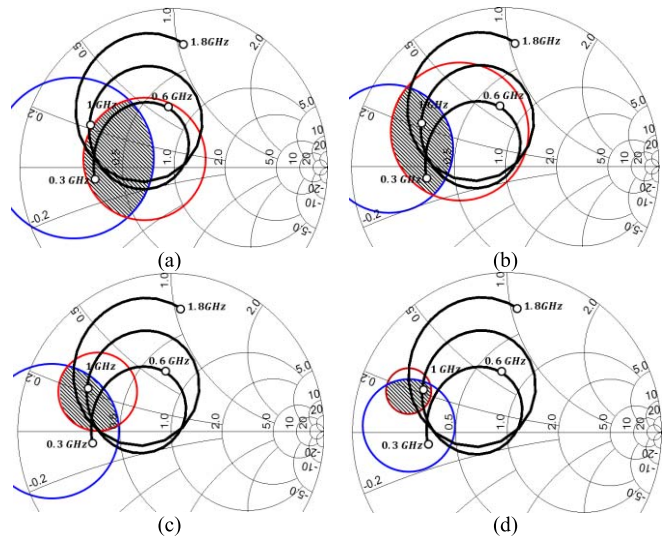

Fig. 6. Input impedance of the first optimal subset. (a) 0.3 GHz. (b) 0.6 GHz. (c) 1 GHz. (d) 1.8 GHz.

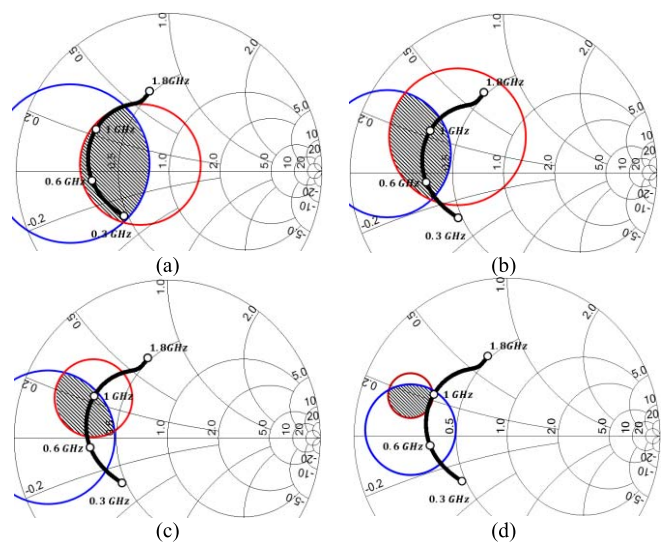

Fig. 7. Input impedance of the second optimal subset. (a) 0.3 GHz. (b) 0.6 GHz. (c) 1 GHz. (d) 1.8 GHz.

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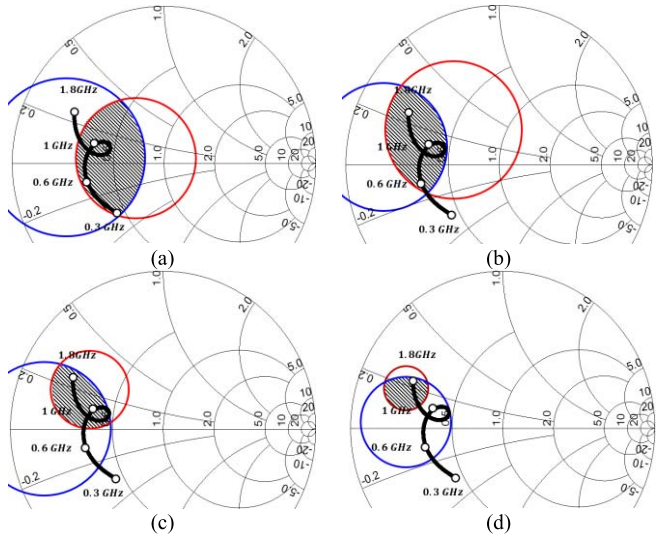

Fig. 8. Input impedance of the third optimal subset. (a) 0.3 GHz. (b) 0.6 GHz. (c) 1 GHz. (d) 1.8 GHz.

and capacitive open stubs should satisfy

$$\omega L = Z_L \sin\left(\frac{2\pi l_L}{\lambda_{gL}}\right) + Z_C \tan\left(\frac{\pi l_C}{\lambda_{gC}}\right) \quad (5)$$

$$\omega C = Z_C \sin\left(\frac{2\pi l_C}{\lambda_{gC}}\right) + \frac{2}{Z_L} \tan\left(\frac{\pi l_L}{\lambda_{gL}}\right) \quad (6)$$

where L and C are the lumped element values for inductors and capacitors from Table I, λ_{gL} and λ_{gC} are the guided wavelengths for high-impedance transmission lines and open stubs, respectively. They can be calculated by equations provided in [32]. The OMN is implemented on a Rogers 4350B substrate with a thickness of 1.52 mm, $\varepsilon_r = 3.48$ and a copper thickness of 35 μm. The realized distributed-element OMN was further optimized to achieve the predefined optimal performance. The implemented OMN layout and corresponding size are illustrated in Fig. 9(a). The fabricated OMN is shown in Fig. 9(b) and the comparison between the measured and simulated OMN input impedance is shown in Fig. 9(c). A 50-Ω transmission line is cascaded to the dc-blocking capacitor to connect it to an SMA connector. For the IMN, the same procedure used to design and implement the OMN was used.

IV. PA Fabrication and Measurement

The PA is realized by connecting the IMN and OMN to the gate and the drain of the transistor, respectively. Importantly, the stability of the PA should be taken into consideration. dc power supplies for the gate and the drain of the transistor are connected by 22-nH inductors to prevent the leakage of RF into dc. A 100-Ω resistor is added in parallel with the inductor of the gate dc supply trail to improve the stability of the amplifier. A photograph of the fabricated PA and the measurement setup is shown in Fig. 10.

The simulated voltage and current waveforms on the intrinsic drain at 0.6 and 1.3 GHz are shown in Fig. 11. The input power level is 30 dBm. The overlap between the voltage and current is relatively small which indicates that the PA can achieve high-efficiency performance.

The fabricated PA has been measured with a continues-wave (CW) signal to examine the large signal performance.

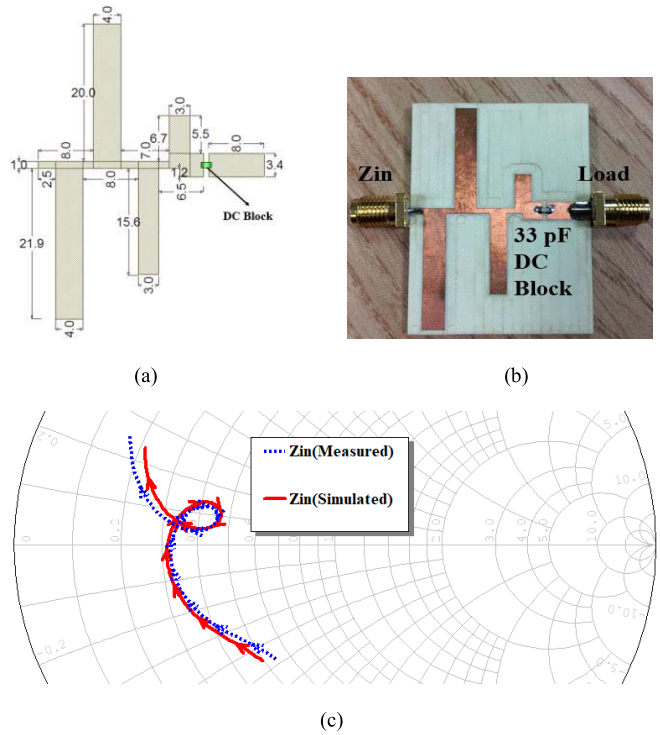

Fig. 9. OMN. (a) Implemented OMN. (b) Fabricated OMN. (c) Comparison between the measured and simulated OMN input impedance.

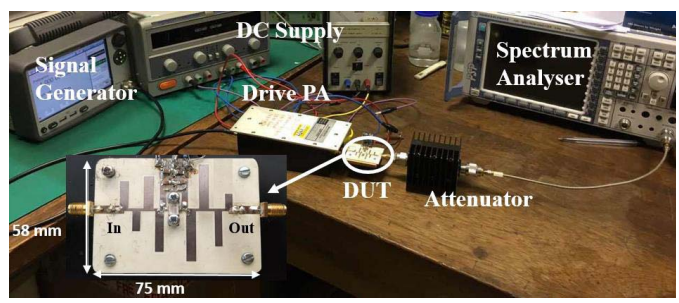

Fig. 10. Photograph of the fabricated PA and the measurement setup.

A single-tone signal was generated by a Keithley 2920 RF signal generator. Due to that the input power required by the PA is up to 32 dBm, a buffer amplifier was used to boost the input power. The output power of the designed PA was measured using a power meter (Rohde & Schwarz NRP-Z85).

The PA was designed to achieve a PAE better than 60% and an output power higher than 42 dBm from 0.2 to 1.8 GHz. To verify the proposed design method, the PA is first measured across the band with 28 V drain voltage, −3.2-V gate voltage and a sweeping input power. The measured PAE and output power are illustrated versus the input power in Figs. 12 and 13, respectively. It can be seen in Fig. 13 that the output has a trend of being compressed when the input power is greater than 28 dBm and the corresponding PAE is also saturated, as shown in Fig. 12. The design requirement of a PAE better than 60% and the output power higher than 42 dBm can be achieved simultaneously with an input power of 30 dBm.

Then the PA is meausred by sweeping the drain voltage while fixing the the input power and the gate voltage at

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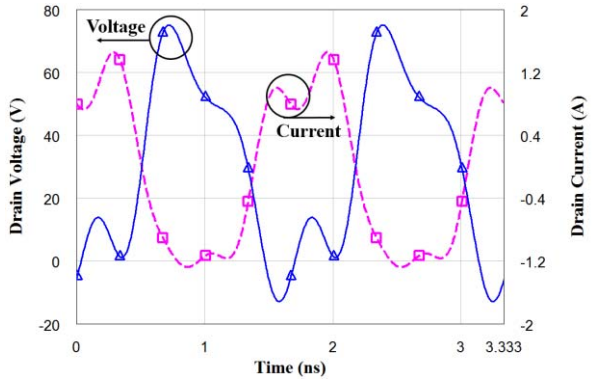
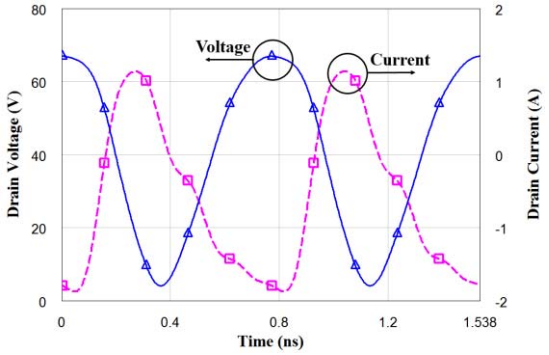


(a)



(b)

Fig. 11. Simulated voltage and current drain waveforms at (a) 0.6 GHz and (b) 1.3 GHz. Measured PAE versus input power at 0.3, 0.6, 0.9, 1.2, 1.5, and 1.8 GHz.

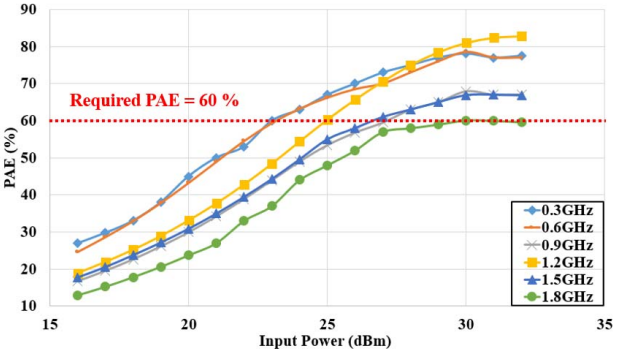


Fig. 12. Measured PAE versus input power at 0.3, 0.6, 0.9, 1.2, 1.5, and 1.8 GHz.

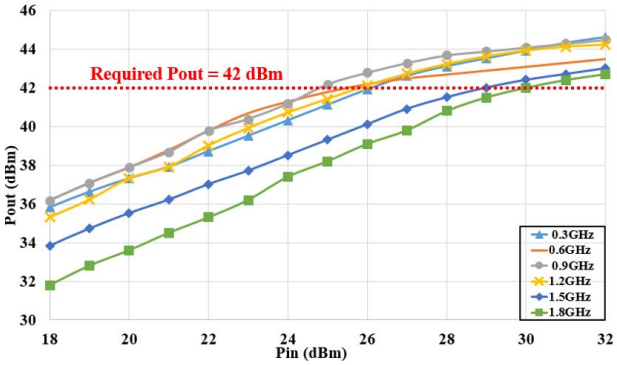


Fig. 13. Measured output power versus input power at 0.3, 0.6, 0.9, 1.2, 1.5, and 1.8 GHz.

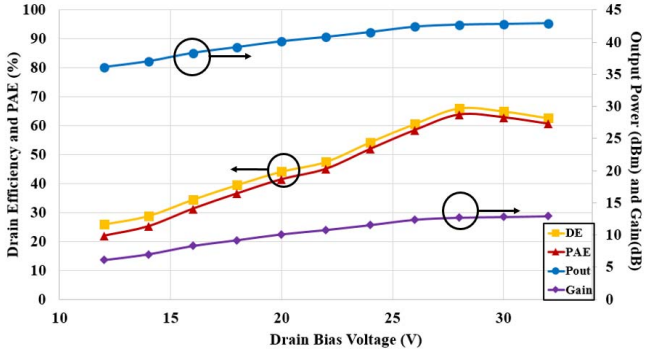


Fig. 14. Measured drain efficiency, PAE, output power, and gain versus drain voltage at 1.3 GHz.

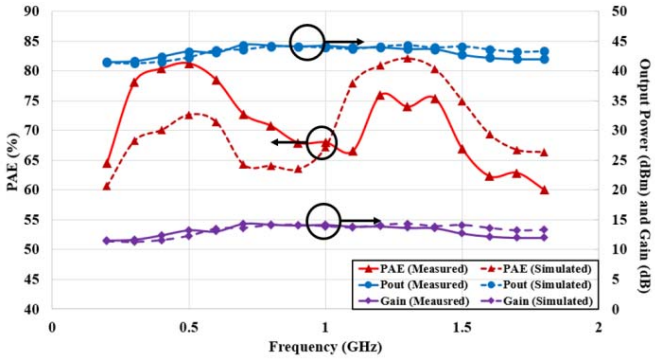


Fig. 15. Comparsion between the measured and simulated PAE, gain, and output power (VDS = 28 V, VGS = −3.2 V and PIN = 30 dBm).

30 dBm and −3.2 V, respectively. Fig. 14 shows the measured result of PAE, output power, and gain versus drain voltage at 1.3 GHz. The maximum PAE (74%) is achieved at 28-V drain voltage.

The comparison between the measured and simulated gain, PAE, and output power is illustrated in Fig. 15. It can be observed that the measured PAE has two peaks which agree with the simulation. The measured PAE is higher than that of the simulation at lower frequencies 0.2–0.9 GHz and is lower at higher frequencies 1.1–1.8 GHz. The difference between the measured and simulated PAE over the band is less than 10%. Also, the trend of simulated and measured output power is consistent with a difference of less than 1.5 dB. This paper has achieved the state-of-the-art performance in terms of bandwidth and efficiency. The comparison with similar broadband PAs is shown in Table II. This PA has achieved a PAE of 60%–82%, an output power of 42–45 dBm (16–32 W) and a gain of 12–15 dB over a frequency band from 0.2–1.8 GHz. This PA has a much wider operational bandwidth compared to those PA with similar efficiency performance, and a higher efficiency compared with those with similar bandwidths. The PA in [6] has achieved a similar efficiency. However, the fractional bandwidth is only 84% (f_H:f_L = 2.4 : 1). The proposed work can achieve the same level of efficiency with a bandwidth of 160% (f_H:f_L = 9 : 1). To the authors' best knowledge, no other work has achieved high efficiency with such a wide bandwidth. The achieved operation bandwidth and efficiency of this design is better than all other work reported so far.

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TABLE II
PERFORMANCE OF STATE-OF-THE-ART BROADBAND HIGH-EFFICIENCY PAs

Ref.	Frequency (GHz)	FBW, f_H:f_L	Gain (dB)	P_{out} (W)	Efficiency (%)
[23]	1.9-4.3	78%, 2.3:1	9-11	10-15	57-72*
[2]	0.36-0.79	81%, 2.2:1	5-14	10	30-81^
[6]	0.9-2.2	84%, 2.4:1	10-13	10-20	63-89*
[12]	1.3-3.3	87%, 2.5:1	10-13	10-11	59-79^
[25]	0.9-3.2	112%, 3.6:1	10-14	9.1-20.4	52-85^
[26]	0.8-4	133%, 5.0:1	5-7	1-2	40-55*
This work	0.2-1.8	160%, 9.0:1	12-15	16-32	60-82^

*: Drain Efficiency, ^: Power Added Efficiency

The bandwidth is defined based on the lowest PAE achieved in this table.

V. CONCLUSION

Owing to the variation of optimal impedances for high PAE across a wide bandwidth, the design methods of the MN reported in the literature require an initial guess, data training, or complex optimization algorithms which significantly increase the design difficulty. This paper has presented a general method to design frequency varying impedances MN s which can be applied to the design of broadband high-efficiency PAs. The wide frequency band has been divided into several frequency sections based on the optimal impedance over the band. The optimal source and load impedances for a transistor have been defined by optimal impedance regions at different frequency sections instead of a fixed value at the center of the desired band. A low-pass *LC*-ladder network has been applied to match the predefined optimal impedance regions. The simplification of the design and optimization of the MNs have been made possible by using the SROM and Voronoi partition. The designed PA has been fabricated and measured to validate the proposed method. The large signal experimental results have shown a PAE of 60%–82%, a gain of 12–15 dB and an output power between 42–45 dBm (16–32 W) over a 160% fractional bandwidth from 0.2 to 1.8 GHz. The state-of-the-art performance is better than any previous reported work. The results have demonstrated the potential of the proposed method to design high-performance amplifiers for future communication systems.

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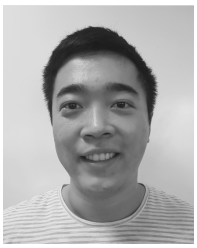
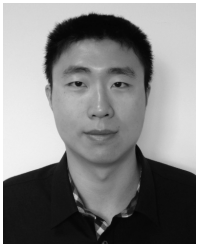


Yuan Zhuang (GS'16) was born in Baoding, China, in 1991. He received the B.Eng. (Hons.) degree in telecommunication engineering from Xi'an Jiao Tong Liverpool University, Suzhou, China, and the University of Liverpool, Liverpool, U.K., in 2014, where he is currently pursuing the Ph.D. degree at the Department of Electrical Engineering and Electronics.

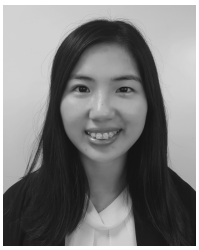
His current research interests include microwave power amplifiers, filters, electromagnetic energy harvesting, and wireless power transfer.



Zhouxiang Fei was born in Xi'an, China, in 1990. He received the B.Eng. degree in electronics and information engineering from Northwestern Polytechnical University, Xi'an, China, in 2012, and the M.Sc. (with distinction) degree in wireless communications from the University of Southampton, Southampton, U.K., in 2013. He is currently pursuing the Ph.D. degree at the University of Liverpool, Liverpool, U.K.

His current research interests include numerical and experimental studies of crosstalk in complex cable bundles with a particular emphasis on considering parameter variability using efficient statistical approaches.

Dr. Fei was a recipient of a student scholarship from the IEEE EMC Society to attend the 2016 IEEE International Symposium on EMC, Ottawa, ON, Canada, 2016. He was also selected as the Best EMC Paper Finalist for the 2016 IEEE International Symposium on EMC.



Anqi Chen received the joint B.Eng. degree in telecommunication engineering from Xi'an Jiao Tong Liverpool University, Suzhou, China, and electrical electronics engineering from the University of Liverpool, Liverpool, U.K., in 2014. She is currently pursuing the Ph.D. degree in electrical and electronic engineering at the University of Liverpool, Liverpool, U.K.

Her current research interests include millimeter-wave filters, broadband power dividers, tunable power dividers and microwave components.

Yi Huang (S'91–M'96–SM'06) received the B.Sc. degree in physics from Wuhan University, Wuhan, China, in 1984, the M.Sc.(Eng.) degree in microwave engineering NRIET, Nanjing, China, in 1987, and the D.Phil. degree in communications from the University of Oxford, Oxford, U.K., in 1994.

He has been conducting research in the areas of wireless communications, applied electromagnetics, radar, and antennas since 1987. He was with NRIET, as a Radar Engineer and spent various periods with the Universities of Birmingham, Oxford, and Essex, U.K. as a Member of Research Staff. In 1994, he joined British Telecom Labs, as a Research Fellow. In 1995, he joined the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, U.K., as a faculty member, where he is currently a Full Professor in Wireless Engineering, the Head of the High Frequency Engineering Group and Deputy Head of Department. He has authored over 300 refereed papers in leading international journals and conference proceedings, and authored *Antennas: From Theory to Practice* (Wiley, 2008) and *Reverberation Chambers: Theory and Applications to EMC and Antenna Measurements* (Wiley, 2016).

Prof. Huang is a Senior Fellow of the HEA. He is a Fellow of the IET. He has received many research grants from research councils, government agencies, charity, EU and industry, acted as a consultant to various companies, and served on a number of the national and international technical committees and has been an Editor, Associate Editor, or Guest Editor of four international journals. He has been a keynote/invited speaker and organizer of many conferences and workshops (e.g., WiCom 2006, 2010, IEEE iWAT2010, and LAPC2012). He is currently the Editor-in-Chief of *Wireless Engineering and Technology*, Associate Editor of IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS, U.K., and Ireland Rep to the European Association of Antenna and Propagation (EurAAP).

Khondker Rabbi received the M.Sc. degree in broadband communications and Ph.D. degree in RF and microwave engineering from the University of Westminster, London, U.K., in 2009 and 2014, respectively.

In 2015, he joined Federal de Santa Catarina University, Florianópolis, Brazil, as a Post-Doctoral Research Fellow, where he designed wireless power transmitters for implantable fully integrated CMOS receivers. Since 2015, he has been a KTP Associate with the University of Liverpool, Liverpool, U.K., where he is involved in designing high-efficiency linear envelope tracking power amplifiers for OFDM systems. His current research interests include nonlinear characterization and modeling of active devices, as well as the design of power RF/microwave amplifiers, high-efficiency transmitting architectures and RF dc/dc power converters.

Jiafeng Zhou received the B.Sc. degree in radio physics from Nanjing University, Nanjing, China, in 1997, and the Ph.D. degree from the University of Birmingham, Birmingham, U.K., in 2004. His doctoral research concerned high-temperature superconductor microwave filters.

From 1997 to 1999, he was with the National Meteorological Satellite Center of China, Beijing, China, where he was involved in the development of communication systems for Chinese geostationary meteorological satellites. From 2004 to 2006, he was a Research Fellow with the University of Birmingham, where his research concerned phased arrays for reflector observing systems. He then joined the Department of Electronic and Electrical Engineering, University of Bristol, Bristol, U.K., where he remained until 2013. His research with the University of Bristol concerned the development of highly efficient and linear amplifiers. He is currently with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, U.K. His current research interests include microwave power amplifiers, filters, electromagnetic energy harvesting, and wireless power transfer.